W800 chip specification

V3.0

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1 Overview

The W800 chip is a secure IoT Wi-Fi/Bluetooth dual-mode SoC chip. Support 2.4G IEEE802.11b/g/n Wi-Fi communication protocol; support BT/BLE dual-mode working mode, support BT/BLE4.2 protocol. The chip integrates 32-bit CPU processor, built-in UART, GPIO, SPI, SDIOÿI ²CÿI ²S, 7816, ADC, TouchSensor and other digital interfaces; support TEE security engine, support a variety of hardware encryption and decryption algorithms, built-in DSP, floating point unit and security engine, support code security permission setting, built-in 2MBFlash memory, support firmware encryption storage, Multiple security measures such as firmware signature, security debugging, and security upgrade ensure product security features. It is suitable for a wide range of Internet of Things fields such as smart home appliances, smart homes, smart toys, wireless audio and video, industrial control, and medical monitoring.

2 features

ÿ Chip Appearance

- ÿ QFN32 package, 4mm x 4mm

ÿ MCU Features

- ÿ Integrated 32-bit XT804 processor, operating frequency 240MHz, built-in DSP, floating point unit and security engine
- ÿ Built-in 2MB Flash, 288KB RAM
- ÿ Integrated PSRAM interface, supports up to 64MB external PSRAM memory
- ÿ Integrated 5-way UART high-speed interface
- ÿ Integrated 2-channel 12-bit ADC, the highest sampling rate is 1KHz
- ÿ Integrates a high-speed SPI interface, supporting up to 50MHz
- ÿ Integrate 1 SDIO_HOST interface, support SDIO2.0, SDHC, MMC4.2
- ÿ Integrate 1 SDIO_DEVICE, support SDIO2.0, the highest throughput rate is 200Mbps
- ÿ Integrated 1 I ²C controller
- ÿ Integrated GPIO controller, supports up to 18 GPIOs
- ÿ Integrated 5-way PWM interface
- ÿ Integrated 1-way Duplex I ²S controller
- ÿ Integrated 11 Touch Sensors

ÿ Security features

- ÿ MCU built-in Tee security engine, the code can distinguish safe world/non-safe world
- ÿ Integrated SASC/TIPC, memory and internal modules/interfaces can be configured with security attributes to prevent non-secure code access
- ÿ Enable firmware signature mechanism to achieve secure Boot/upgrade
- ÿ Equipped with firmware encryption function to enhance code security
- ÿ Firmware encryption keys are distributed using asymmetric algorithms to enhance key security
- ÿ Hardware encryption module: RC4256, AES128, DES/3DES, SHA1/MD5, CRC32, 2048 RSA, true random number generator

ÿ Wi-Fi characteristics

- ÿ Support GB15629.11-2006, IEEE802.11 b/g/n
- ÿ ÿÿ Wi-Fi WMM/WMM-PS/WPA/WPA2/WPS

ÿ Support EDCA channel access method

ÿ Support 20/40M bandwidth working mode

ÿ Support STBC, GreenField, Short-GI, support reverse transmission

ÿ Support AMPDU, AMSDU

ÿ Support IEEE802.11n MCS 0~7, MCS32 physical layer transmission rate stalls, the maximum transmission rate is 150Mbps

ÿ Support Short Preamble when sending at 2/5.5/11Mbps

ÿ Support HT-immediate Compressed Block Ack, Normal Ack, No Ack response mode

ÿ Support CTS to self

ÿ Support Station, Soft-AP, Soft-AP/Station functions

ÿ Bluetooth Features

ÿ Integrated Bluetooth baseband processor/protocol processor, supports BT/BLE dual-mode working mode, supports BT/BLE4.2 protocol

ÿ Low power mode ÿ

3.3V single power supply ÿ

Support Wi-Fi power saving mode power management

ÿ Support work, sleep, standby, shutdown working modes ÿ

Standby power consumption is less than 10uA

3 chip structure

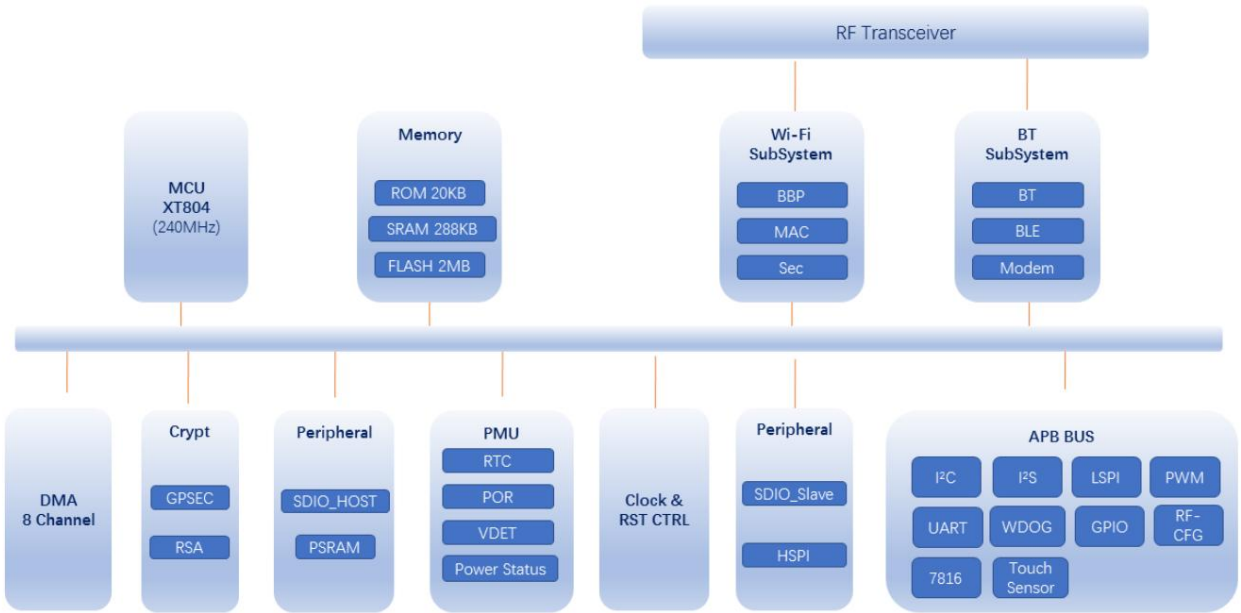

Figure 3-1 W800 chip structure diagram

4 Address space division

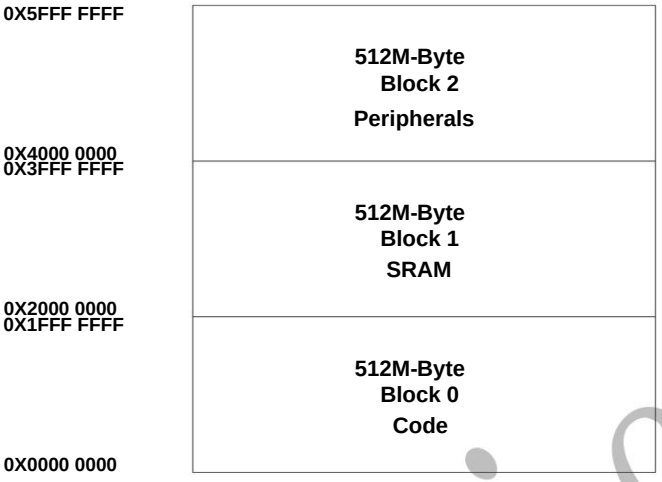

Figure 4-1 Address space mapping

Table 4-1 Detailed division of bus device address space

bus slave	BootMode=0	Address Space Subdivision	Remark
ROM	0x0000 0000 - 0x0004 FFF		Store the solidified firmware code
FLASH	0x0800 0000 - 0x0FFF FFFF		as a dedicated instruction memory.
SRAM	0x2000 0000 - 0x2002 7FFF		Firmware memory and instruction store
Mac RAM	0x2002 8000 - 0x2004 7FFF		SDIO/H-SPI/UART data buffer
PSRAM	0x3000 0000 - 0x30800000		peripheral memory
CONFIG	0x4000 0000 - 0x4000 2FFF 0x4000 0000	- 0x4000 05FF RSA configuration space	
		0x4000 0600 - 0x4000 07FF GPSEC configuration space	
		0x4000 0800 - 0x4000 09FF DMA configuration space	
		0x4000 0A00 - 0x4000 0CFF SDIO_HOST configuration space	
		0x4000 0D00 - 0x4000 0DFF PMU configuration space	
		0x4000 0E00 - 0x4000 0EFF Clock and Reset configuration space	
		0x4000 0F00 - 0x4000 0FFF MacPHY Router configuration space	
		0x4000 1000 - 0x4000 13FF BBP configuration space	
		0x4000 1400 - 0x4000 17FF MAC configuration space	
		0x4000 1800 - 0x4000 1FFF SEC configuration space	
		0x4000 2000 - 0x4000 21FF FLASH Controller configuration space	
		0x4000 2200 - 0x4000 23FF PSRAM_CTRL configuration space	
		0x4000 2400 - 0x4000 25FF SDIO Slave configuration space	
		0x4000 2600 - 0x4000 27FF H-SPI configuration space	

		0x4000 2800	0x4000 29FF	SD Wrapper configuration space
		0x4000 2A00	0x4000 A9FF	BT Core configuration space
		0x4000 B000	0x4000 B0FF	SASC-B1 Level 1 bus memory security configuration module
		0x4000 B100	0x4000 B1FF	SASC-Flash Flash security configuration module
		0x4000 B200	0x4000 B2FF	SASC-B2 secondary bus memory security configuration module
APB	0x4001 0000 – 0x4001 C000	0x4001 0000	0x4001 01FF	I²C master
		0x4001 0200	0x4001 03FF	Sigma ADC
		0x4001 0400	0x4001 07FF	SPI master
		0x4001 0600	0x4001 07FF	UART0
		0x4001 0800	0x4001 09FF	UART1
		0x4001 0A00	0x4001 0BFF	UART2
		0x4001 0C00	0x4001 0DFF	UART3
		0x4001 0E00	0x4001 0FFF	UART4
		0x4001 1000	0x4001 11FF	
		0x4001 1200	0x4001 13FF	GPIO-A
		0x4001 1400	0x4001 15FF	GPIO-B
		0x4001 1600	0x4001 17FF	WatchDog
		0x4001 1800	0x4001 19FF	Timer
		0x4001 1A00	0x4001 1BFF	RF_Controller
		0x4001 1C00	0x4001 1DFF	
		0x4001 1E00	0x4001 1FFF	PWM
		0x4001 2000	0x4001 22FF	I²S
		0x4001 2200	0x4001 23FF	BT-modem
		0x4001 2400	0x4001 25FF	Touch Sensor
		0x4001 2600	0x4001 25FF	TIPC Interface Security Settings
		0x4001 4000	0x4000 BFFF	RF_BIST DAC transmit memory
		0x4001 C000	0x4003 BFFF	RF_BIST ADC receive memory
		0x4001 3C00	0x5FFF FFFF	RSV

5 Functional description

5.1 SDIO HOST controller

The SDIO HOST device controller provides a digital interface capable of accessing Secure Digital Input Output (SDIO) and MMC cards. Able to access SDIO devices and SD card devices compatible with SDIO 2.0 protocol. The main interfaces are CK, CMD and 4 data lines. ÿ Compatible with SD Card Specification 1.0/1.1/2.0(SDHC)

ÿ Compatible with SDIO Memory Card Specification 1.1.0

ÿ Compatible with MMC specification 2.0~4.2

ÿ Configurable interface clock rate, support host rate 0~50MHz

ÿ Support standard MMC interface

ÿ Support up to 1024 bytes Block

ÿ Support soft reset function

ÿ Automatic Command/Response CRC generation/verification

ÿ Automatic data CRC generation/checking

ÿ Configurable timeout detection

ÿ Support SPI, 1-bit SD and 4-bit SD modes

ÿ Support DMA data transfer

5.2 SDIO Device Controller

SDIO2.0 device-side interface to complete the data interaction with the host. Internally integrates 1024Byte asynchronous FIFO to complete the data between the host and the chip interact.

ÿ Compatible with SDIO Card Specification 2.0

ÿ Support host rate 0~50MHz

ÿ Support up to 1024 bytes Block

ÿ Support soft reset function

ÿ Support SPI, 1-bit SD and 4-bit SD modes

5.3 High Speed SPI Device Controller

Compatible with the general SPI physical layer protocol, by agreeing on the data format for interaction with the host, the host can access the device at a high speed, and the maximum supported working frequency is 50Mbps. ÿ Compatible with general SPI protocol

ÿ Selectable level interrupt signal

ÿ Support up to 50Mbps rate

ÿ Simple frame format, full hardware analysis and DMA

5.4 DMA Controller

Support up to 8 channels, 16 DMA request sources, support linked list structure and register control.

ÿ Amba2.0 standard bus interface, 8 DMA channels

ÿ Support DMA operation based on memory linked list structure

ÿ Software configures 16 hardware request sources

ÿ Support 1, 4-burst operation mode

ÿ Support byte, half-word, word operations

ÿ The source and destination addresses are unchanged or sequentially incremented, configurable or cyclically operate within a predefined address range

ÿ Synchronous DMA request and DMA response hardware interface timing

5.5 Clock and Reset

Support chip clock and reset system control, clock control includes clock frequency conversion, clock shutdown and adaptive gating; reset control includes soft reset control of the system and sub-modules.

5.6 Memory Manager

Support the configuration of sending and receiving buffer size, as well as control information such as the base address of MAC access buffer, the number of buffers, and the upper limit of frame aggregation.

5.7 Digital

baseband supports IEEE802.11a/b/g/e/n (1T1R) transmitter and receiver algorithm implementation, main parameters: ÿ Data rate: 1~54Mpbs (802.11a/b/g), 6.5~150Mbps (802.11n)

ÿ MCS format: MCS0~MCS7, MCS32 (40MHz HT Duplicate mode)

ÿ Support 40MHz bandwidth non-HT Duplicate mode, 6Mÿ54M

ÿ Signal bandwidth: 20MHz, 40MHz

ÿ Modulation: DSSS (DBPSK, DQPSK, CCK) and OFDM (BPSK, QPSK, 16QAM, 64QAM)

ÿ Realize 1T1R MIMO-OFDM spatial multiplexing

ÿ Support Short GI mode

ÿ Support legacy mode and Mixed mode

ÿ Support the transmission and reception of 20M upper and lower sideband signals under 40MHz bandwidth

ÿ Support STBC reception of MCS0~7, 32

ÿ Support Green Field mode

5.8 MAC Controller

Support IEEE802.11a/b/g/e/n MAC sublayer protocol control, specific specifications include: ÿ Support EDCA channel access mode

ÿ Support CSMA/CA, NAV and TXOP protection mechanism

ÿ Beacon, Mng, VO, VI, BE, BK five-way sending queue and QoS

ÿ Support single and wide group wave frame receiving and sending

ÿ Support RTS/CTS, CTS2SELF, Normal ACK, No ACK frame sequence

ÿ Support retransmission mechanism and retransmission rate and power control

ÿ Support MPDU hardware aggregation and de-aggregation and Immediate BlockAck mode

ÿ Support RIFSÿSIFSÿAIFS

ÿ Support reverse transfer mechanism

ÿ Support TSF timing, and software configurable

ÿ Support MIB statistics

5.9 Security system

Support the security algorithm stipulated in IEEE802.11a/b/g/e/n protocol, cooperate to complete the encryption and decryption of sending and receiving data frames.

ÿ Satisfied that the encryption and decryption throughput rate is greater than 150Mbps

ÿ Amba2.0 standard bus interface

ÿ Support WAPI Security Mode 2.0

ÿ Support WEP security mode - 64-bit encryption

ÿ Support WEP security mode - 128-bit encryption

ÿ Support TKIP security mode

ÿ Support CCMP security mode

5.10 FLASH controller

ÿ Provide bus access FLASH interface ÿ Provide system bus and data bus access arbitration ÿ Implement CACHE cache system to improve FLASH interface access speed ÿ Provide compatibility with different QFlash

5.11 RSA encryption module

RSA operation hardware coprocessor, providing Montgomery (FIOS algorithm) modular multiplication operation function. Cooperate with RSA software library to realize RSA algorithm. Supports 128-bit to 2048-bit modular multiplication.

5.12 General hardware encryption module

The encryption module automatically completes the encryption of the source address space data of the specified length, and automatically writes the encrypted data back to the specified destination address space after completion; supports SHA1/MD5/RC4/DES/3DES/AES/CRC/TRNG.

ÿ Support SHA1/MD5/RC4/DES/3DES/AES/CRC/TRNG encryption algorithm

ÿ DES/3DES supports both ECB and CBC modes

ÿ AES supports three modes: ECB, CBC and CTR

ÿ CRC supports CRC8, CRC16_MODBUS, CRC16_CCITT and CRC32 four modes

ÿ CRC supports input/output reverse

ÿ SHA1/MD5/CRC supports continuous multi-packet encryption

ÿ Built-in true random number generator, also supports seed seed to generate pseudo-random numbers

5.13 I²C controller

APB bus protocol standard interface, only supports the main device controller, I²C working frequency support can be configured, 100K-400K.

5.14 Master/Slave SPI Controller

Supports synchronous SPI master-slave functionality. Its working clock is the internal bus clock of the system. Its characteristics are as follows:

ÿ 8-word-deep FIFOs for transmit and receive paths

ÿ master supports 4 formats of Motorola SPI (CPOL, CPHA), TI timing, macrowire timing

ÿ slave supports 4 formats of Motorola SPI (CPOL, CPHA);

ÿ Support full duplex and half duplex

ÿ The master device supports bit transmission, up to 65535bit transmission

ÿ The slave device supports transmission modes of various byte lengths

ÿ The maximum clock frequency of SPI_Clk input from the device is 1/6 of the system clock

5.15 UART Controller

ÿ The device conforms to the APB bus interface protocol ÿ
Support interrupt or polling mode of operation ÿ Support
DMA transmission mode, each sending and receiving has 32-byte FIFO ÿ Programmable baud
rate ÿ 5-8bit data length, and configurable parity polarity ÿ 1 or 2 stop bits can be configured ÿ
Support RTS/CTS flow control ÿ Support Break frame sending and receiving ÿ Overrun, parity
error, frame error, rx break frame interrupt indication ÿ Maximum 16-burst byte DMA operation

5.16 GPIO Controller

Configurable GPIO, software-controlled input and output, hardware-controlled input and output, configurable interrupt mode.
The GPIOA and GPIOB registers have different starting addresses, but the functions are the same.

5.17 Timers

Microsecond and millisecond timing (the number of counts is configured according to the clock frequency), and six configurable 32-bit counters are implemented. When the counting configured by the corresponding calculator is completed, a corresponding interrupt is generated.

5.18 Watchdog Controller

Support "watchdog" function. Observe the correctness of software behavior and allow a global reset after a system crash. "Watchdog" generates a periodic interrupt, and the system software must respond to this interrupt and clear the interrupt flag; if the interrupt flag has not been cleared for a long time due to system crash, a hard reset will be generated to reset the system globally.

5.19 RF Configurator

A synchronous SPI master function is implemented. Its working clock is the internal bus clock of the system. Its characteristics are as follows:

ÿ 1-word-deep FIFOs for transmit and receive paths

5.20 RF Transceiver

ÿ The radio frequency transceiver part includes modules including power amplifier, transmit path, receive path, phase-locked loop and SPI. by adjusting Control ports SHDN, RXEN and TXEN to change the working state of the chip

ÿ The receiving path adopts a zero-IF structure, which directly converts the RF signal into two outputs of baseband I and Q. The RF front-end works at 2.4GHz and includes a low-noise amplifier and a quadrature mixer; the baseband is composed of a low-pass filter and a variable gain amplifier to achieve channel filtering and gain control; the drive amplifier provides different DC outputs for the ADC interface

ÿ The transmission path includes: programmable control filter, up-conversion mixer, variable gain amplifier and power amplifier, and the transmission path also adopts a direct conversion structure. The output signal of the DAC passes through a low-pass filter to filter out the image frequency and out-of-band noise. PA output is differential output to drive off-chip antenna

5.21 PWM Controller

ÿ 5-channel PWM signal generation function ÿ 2-channel input signal capture function (PWM0 and PWM4 two channels) ÿ Frequency range: 3Hz~160KHz ÿ Maximum accuracy of duty cycle: 1/256, counter width for inserting dead zone: 8bit

5.22 I²S Controller

ÿ Supports AMBA APB bus interface, 32bit single read and write operations ÿ Supports master and slave modes, can work in duplex ÿ Supports 8/16/24/32 bit width, the highest sampling frequency is 128KHz ÿ Supports mono and stereo modes I²S and MSB justified data format, compatible with PCM A/B format ÿ Support DMA request read and write operations. Only word-by-word operations are supported

5.23 7816/UART Controller

ÿ The device side conforms to the APB bus interface protocol ÿ Support interrupt or polling working mode ÿ Support DMA transmission mode, each sending and receiving has 32-byte FIFO ÿ DMA can only operate by byte, the maximum 16-burst byte DMA operation is compatible with UART and 7816 interface function: Serial port function: ÿ Baud rate programmable ÿ 5-8bit data length, and parity polarity configurable ÿ 1 or 2 stop bits configurable ÿ Support RTS/CTS flow control ÿ Support Break frame sending and receiving ÿ Overrun, parity error, frame error, rx break frame interrupt indication 7816 interface function: ÿ Compatible with ISO-7816-3 T=0.T=1 mode ÿ Compatible with EVM2000 protocol ÿ Configurable guard time (11 ETU-267 ETU) ÿ Positive The direction/reverse agreement can be configured by software ÿ Support send/receive parity and retransmission function ÿ Support 0.5 and 1.5 stop bit configuration

5.24 PSRAM Interface Controller

W800 has a built-in PSRAM controller with SPI/QSPI interface, supports external PSRAM device access, and provides bus-based PSRAM read, write, and erase operations. The highest read and write speed is 80MHz. ÿ Supports read and write access to external PSRAM

ÿ Configurable as SPI and QSPI

ÿ SPI/QSPI clock frequency can be configured

ÿ Support BURST INC mode access

ÿ Support PSRAM semi-sleep mode

5.25 ADC

The acquisition module based on Sigma-Delta ADC completes the acquisition of up to 4 channels of analog signals. The sampling rate is controlled by an external input clock. It can acquire input voltage and chip temperature, and supports input calibration and temperature compensation calibration.

5.26 Touch key controller

The basic functions of the module

are as follows: ÿ Support up to 11 channels of Touch Sensor scanning

ÿ Record the scanning results of each Touch Sensor

ÿ Report scan results through interrupts

6 Pin definition

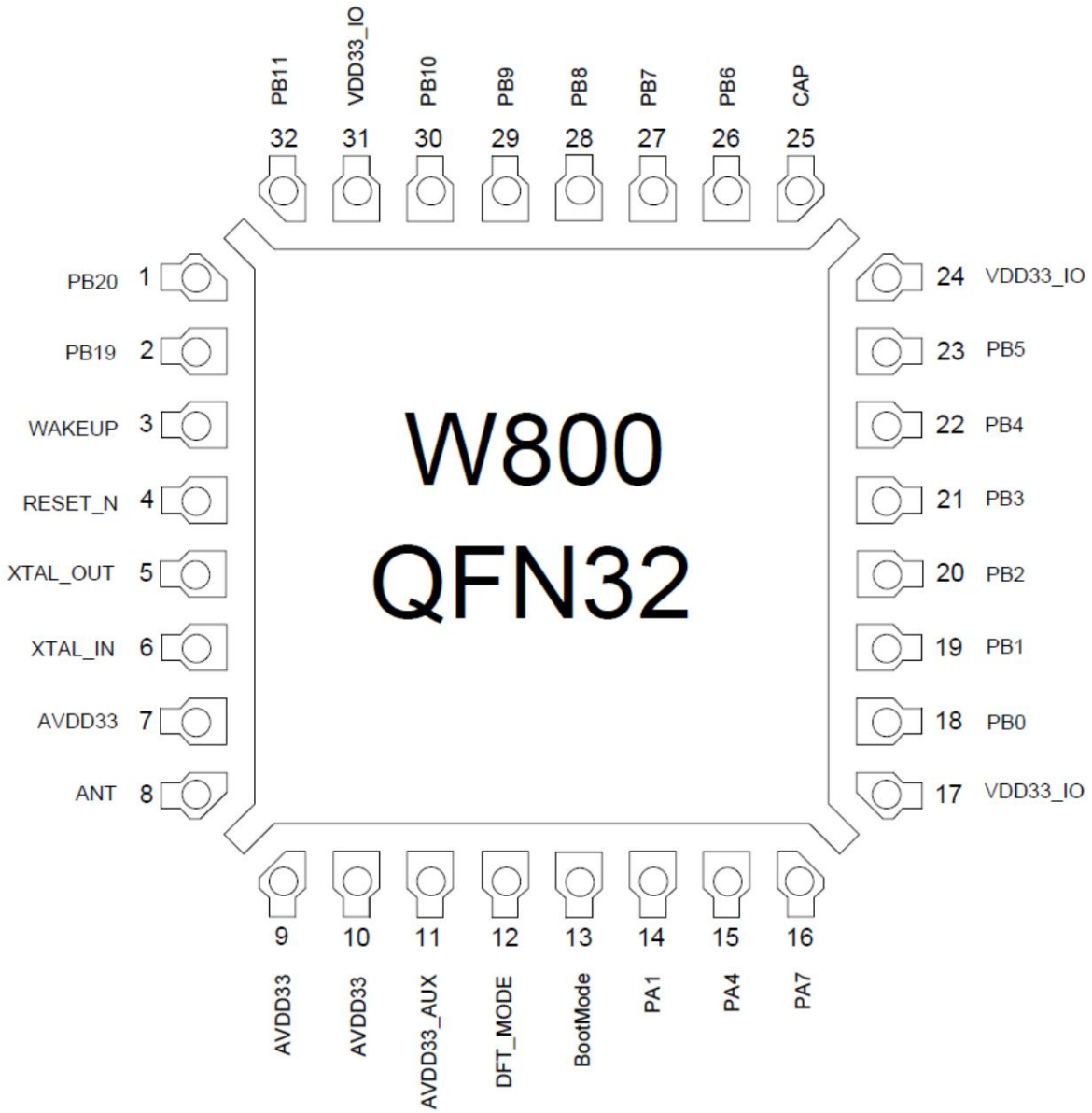

Figure 6-1 Pin layout diagram (QFN32)

Table 6-1 Pin assignment definition (QFN32)

No.	Name	Type	Pin Function After Reset		multiplexing function	Highest frequency	pull-up and pull-down capability	drive capability
1	PB_20	I/O	UART_RX		UART0_RX/PWM1/UART1_CTS/I²C_SCL	10MHz	UP/DOWN	12mA
2	PB_19	I/O	UART_TX		UART0_TX/PWM0/UART1_RTS/I²C_SDA	10MHz	UP/DOWN	12mA

3	WAKEUP	I	WAKEUP wake up function			DOWN	
4	RESET	I	RESET reset			UP	
5	XTAL_OUT	O	External crystal oscillator output				
6	XTAL_IN	I	External crystal oscillator input				
7	AVDD33	P	chip power supply, 3.3V				
8	ON	I/O	RF Antenna				
9	AVDD33	P	chip power supply, 3.3V				
10	AVDD33	P	chip power supply, 3.3V				
11	AVDD33_AUX	P	chip power supply, 3.3V				
12	TEST	I	Test function configuration pin				
13	BOOTMODE	I/O	BOOTMODE	I²S_MCLK/LSPI_CS/PWM2/I²S_DO	20MHz	UP/DOWN	12mA
14	PA_1	I/O	JTAG_CK	JTAG_CK/I²C_SCL/PWM3/I²S_LRCK/ADC0	20MHz	UP/DOWN	12mA
15	PA_4	I/O	JTAG_SWO	JTAG_SWO/I²C_SDA/PWM4/I²S_BCK/ADC1	20MHz	UP/DOWN	12mA
16	PA_7	I/O	GPIO, input, high impedance	PWM4/LSPI_MOSI/I²S_MCK/I²S_DI /Touch0	20MHz	UP/DOWN	12mA
17	VDD33IO	P	IO power supply, 3.3V				
18	PB_0	I/O	GPIO, input, high impedance	PWM0/LSPI_MISO/UART3_TX/PSRAM_CK/To uch3	80MHz	UP/DOWN	12mA
19	PB_1	I/O	GPIO, input, high impedance	PWM1/LSPI_CK/UART3_RX/PSRAM_CS/Touc h4	80MHz	UP/DOWN	12mA
20	PB_2	I/O	GPIO, input, high impedance	PWM2/LSPI_CK/UART2_TX/PSRAM_D0/Touc h5	80MHz	UP/DOWN	12mA
21	PB_3	I/O	GPIO, input, high impedance	PWM3/LSPI_MISO/UART2_RX/PSRAM_D1/To three6	80MHz	UP/DOWN	12mA
22	PB_4	I/O	GPIO, input, high impedance	LSPI_CS/UART2_RTS/UART4_TX/PSRAM_D2 /Touch7	80MHz	UP/DOWN	12mA
23	PB_5	I/O	GPIO, input, high impedance	LSPI_MOSI/UART2_CTS/UART4_RX/PSARM_ D3/Touch8	80MHz	UP/DOWN	12mA
24	VDD33IO	P	IO power supply, 3.3V				
25	CAP	I	External capacitor, 4.7μF				
26	PB_6	I/O	GPIO, input, high impedance	UART1_TX/MMC_CLK/HSPI_CK/SDIO_CK/To uch9	50MHz	UP/DOWN	12mA
27	PB_7	I/O	GPIO, input, high impedance	UART1_RX/MMC_CMD/HSPI_INT/SDIO_CMD/ Touch10	50MHz	UP/DOWN	12mA
28	PB_8	I/O	GPIO, input, high impedance	I²S_BCK/MMC_D0/PWM_BREAK/SDIO_D0/ Touch11	50MHz	UP/DOWN	12mA
29	PB_9	I/O	GPIO, input, high impedance	I²S_LRCK/MMC_D1/HSPI_CS/SDIO_D1/ Touch12	50MHz	UP/DOWN	12mA
30	PB_10	I/O	GPIO, input, high resistance	I²S_DI/MMC_D2/HSPI_DI/SDIO_D2	50MHz	UP/DOWN	12mA

31	VDD33IO	P	IO power supply, 3.3V				
32	PB_11	I/O GPIO, input, high-impedance I²S_DO/MMC_D3/HSPI_DO/SDIO_D3			50MHz	UP/DOWN	12mA
33	GND	P ground					

Note: 1. I = Input, O = Output, P = Power

7 Electrical Characteristics

7.1 Limit parameters

Table 7-1 Typical values of

	name minimum		limit parameters	maximum value	unit
Parameter Supply	VDD	3.0	3.3	3.6	IN
Voltage Input Logic Level	WILL	-0.3		0.8	IN
Low Input Logic Level High	HIV	2.0		VDD+0.3	IN
Input Pin Capacitance	cpad			2	pF
Output Logic Level Low	VOL			0.4	IN
Output Logic Level High	VOH	2.4			IN
Output Maximum Drive Capacity	IMAX			24	mA
Storage Temperature Range	TSTR	-40ÿ		+125ÿ	ÿ
Operating Temperature Range	TOPR	-40ÿ		+85ÿ	ÿ

7.2 RF Power Consumption Parameters

Test conditions: 3.3V power supply, transmit according to 50% duty cycle test. Table

7-2 RF power consumption parameters

Mode	typical value	unit
Transmit IEEE802.11b 1Mbps POUT = +19.4dBm	240	mA
Transmit IEEE802.11b 11Mbps POUT = +19.3dBm	240	
Transmit IEEE802.11g 54Mbps POUT = +14.7 dBm	190	mA
Send IEEE802.11n MCS7 POUT = +12dBm	180	mA
Receive IEEE802.11b/g/n	95	mA

7.3 Wi-Fi shooting

Table 7-3 Wi-Fi radio parameters

parameter	typical value	unit
input frequency	2.4~2.4835	GHz
transmit power		
IEEE802.11b 11Mbps	19±2	dBm
IEEE802.11g 54Mbps	16±2	dBm
IEEE802.11n MCS7 HT20	13±2	dBm

Receiver sensitivity		
IEEE802.11b 1Mbps	-96	dBm
IEEE802.11b 11Mbps	-87	dBm
IEEE802.11g 54Mbps	-73	dBm
IEEE802.11g MCS7 HT20	-71	dBm
Adjacent channel inhibition		
IEEE802.11b 6Mbps	32	dB
IEEE802.11g 54Mbps	16	dB
IEEE802.11n HT20, MCS0	31	dB
IEEE802.11n HT20, MCS7	12	dB

7.4 Bluetooth RF

7.4.1 Traditional Bluetooth RF

Receiver - Base Data Rate (BR)

	condition	Min Typ Max Unit			
Parameter Sensitivity@0.1%			-91		dBm
BER Maximum Received Signal@0.1%			0		dBm
BER Co-Channel Rejection Ratio C/I Out-			9		dB
of-Band Blocking	30 MHz 2000 MHz		-10		dBm
	2000 MHz 2400 MHz		-27		dBm
	2500 MHz 3000 MHz		-27		dBm
	3000 MHz 12.5 GHz		-10		dBm
Intermodulation			-39		dB

Emitter - Base Rate (BR)

	condition	Min Typ Max Unit			
Parameters RF			6		dBm
Transmit Power Gain			3		db
Control Step Size RF Power		-10		12	dBm
Control Range 20 dB Bandwidth		0.918 0.923			
ÿ f1avg			159.8		
ÿ f2max			142.8		
ÿ f2avg/ÿ f1avg			0.89		
ICFT			0		

Drift Rate Offset		-2.25 -2.08 2.23			kHz
(DH1) Offset (DH5)		-4		-1	kHz
			0	21	kHz

Receiver - Enhanced Rate (EDR)

Parameter ÿ/4 DQPSK Sensitivity @	condition	Min Typ Max Unit			
0.01% BER Maximum Received					
Signal @ 0.01% BER			-88		dBm
			0		dBm
8DPSK					
Sensitivity@0.01% BER Maximum			-81		dBm
Received Signal@0.01% BER			0		dBm

Transmitter - Enhanced Data Rate (EDR)

	condition	Min Typ Max Unit			
Parameter RF transmit			0		dBm
power gain control step			3		db
RF power control range ÿ/4		-10		8	dBm
DQPSK max w0 ÿ/4 DQPSK		-3.2		2.6	KHz
max wi ÿ/4 DQPSK max |wi +		-5.3		-2.4	KHz
w0|		-4.8		-3.9	KHz
8DPSK max w0		-1.4		1.5	KHz
8DPSK max wi		-4.1		-2.9	KHz
8DPSK max |wi + w0| ÿ/4 DQPSK		-4.8		-4.1	KHz
modulation accuracy RMS DEVM			6.7		%
	99% DEVM		100		%
	Peak DEVM		14.1		%
8 DPSK modulation accuracy	RMS DEVM		6.8		%
	99% DEVM		99.99		%
	Peak DEVM		15.3		%
EDR differential phase encoding			100		%

7.4.2 Bluetooth Low Energy Radio

Receiver

	condition	Min Typ Max Unit			
Parameters Sensitivity @30.8%			-94		dBm
PER Maximum Received Signal @30.8%				0	dBm
PER Out-of-Band Blocking	30MHz~2000MHz		-30		dBm
	2003MHz~2399MHz		-35		dBm
	2484MHz~3000MHz		-35		dBm

	3000MHz~12.5GHz		-30		dBm
Intermodulation			-47		dBm

Transmitter

	condition	Min Typ Max Unit			
Parameters RF			6		dBm
Transmit Power Gain			2		db
Control Step Size RF Power Control Range		-10		12	dBm
ÿ f1avg		240.8	241.2 242		kHz
ÿ f2max		175.7	182.7 183.9	kHz	
drift rate offset			1.5		kHz
			-4.3		kHz

8 Package Information

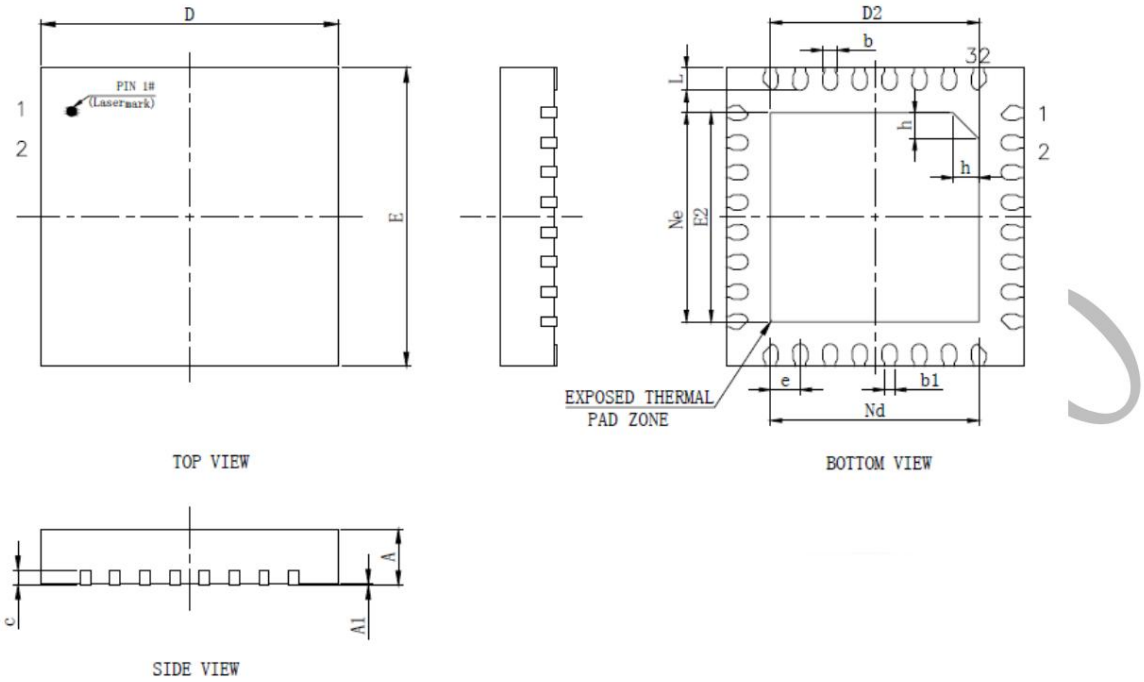

Figure 8-1 W800 package parameters

Table 8-1 W800 Package Parameters

SYMBOL	MILLIMETER		
	MIN	NAME	MAX
A	0.70	0.75	0.80
A1	0.00	0.02	0.05
b	0.15	0.20	0.25
c	0.18	0.20	0.25
D	3.90	4.00	4.10
D2	2.70	2.80	2.90
and	0.40BSC		
Yes	2.80BSC		
Nd	2.80BSC		
AND	3.90	4.00	4.10
E2	2.70	2.80	2.90
L	0.25	0.30	0.35
h	0.30	0.35	0.40
L/F carrier size	122x122		