Overview

The CST816D self-capacitive touch chip uses a high-speed MCU core and an embedded DSP circuit. Combined with its own fast self-capacitive sensing technology, it can widely support a variety of self-capacitive patterns including triangles, and implement single-point gestures and real two-point operations on it, achieving extremely high sensitivity and low standby power consumption.

Chip Features

ÿ Built-in fast self-capacitance detection circuit and high-performance DSP module

ÿ Support online programming; ÿ Built-in watchdog; ÿ Support multiple buttons; ÿ Support standby gesture wake-up function;

ÿ Capacitive screen support

ÿ Supports up to 13 sensing channels; ÿ Supports channel suspension/pull-down design; ÿ Automatic adjustment of module parameters;

ÿ Performance indicators

ÿ Refresh rate > 100Hz; ÿ Single-point gesture and real two-point operation;

ÿ Power consumption index

ÿ Typical power consumption in dynamic mode is 4mA; ÿ Typical power consumption in sleep mode is 8uA;

ÿ Communication interface

ÿ I2C master/slave communication interface, rate 10Khz~400Khz Configurable;

ÿ Compatible with 1.8V/3.3V interface levels.

ÿ Power supply

ÿ Single power supply 2.8V ~ 3.6V, power ripple <= 50mvÿ

ÿ Package type: QFNWB3*3-20L(P0.4T0.55ÿ

Application

For products such as bracelets and watches, the TP size is recommended to be within 1.8 inches.

References

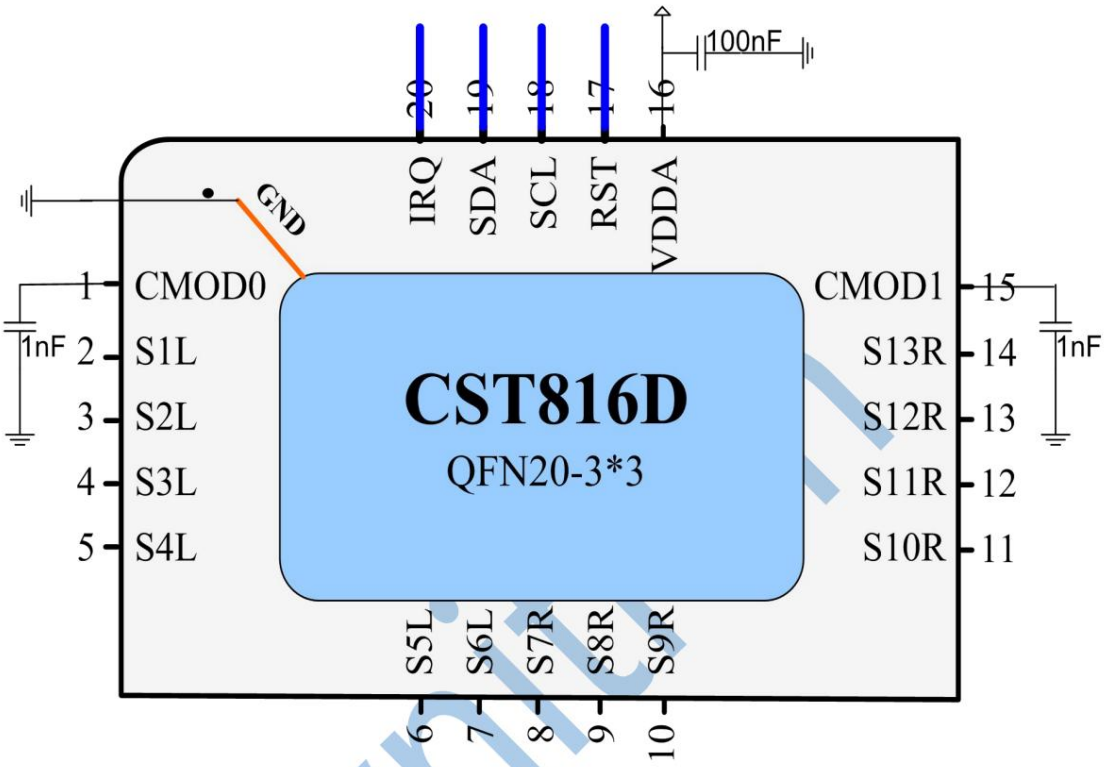


Figure 1. Reference Circuit Diagram

Note:

ÿ CMOD filter capacitors use NPO/COG material capacitors with at least 10% accuracy. ÿ The selection range of CMOD capacitance value is between 1nF and 5.6nF, and 1nF is generally selected. The specific optimal value is related to the corresponding body capacitance. ÿ CMOD filter capacitors must be placed close to the corresponding pins of the chip, and the traces between the chip should be as short as possible.

Ordering Information

Part Number	Encapsulation	Surface printing	Package
CST816D	QFNWB3*3-20L(P0.4T0.55ÿ	CST816D XXXXXXXXX (Production tracking code)	Taping (5000)

surface *1:* Ordering Information

Pinout/Description

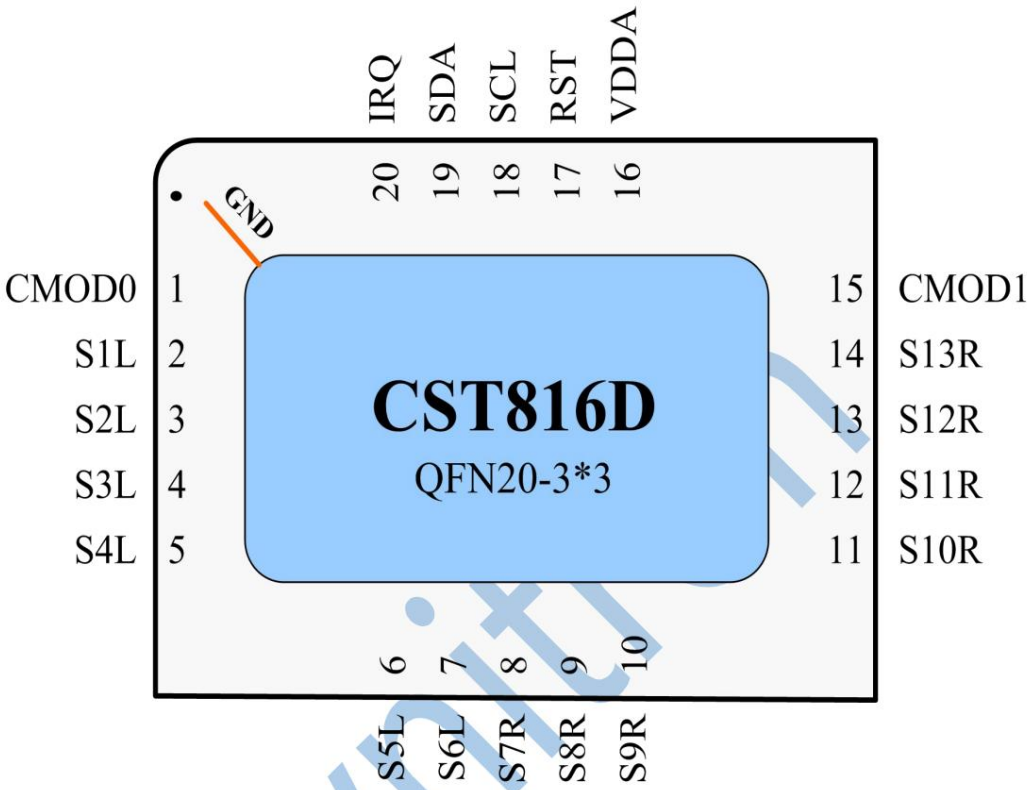


Figure 2. Pin Description

name		Remark
S01~S13	**Description** Sensing channel	
VDDA	power supply	2.8V~3.6V, connected to 2.2uF~10uF capacitor
CMOD0/CMOD1 voltage stabilizing capacitor		Connect 1nF~5.6nF voltage stabilizing capacitor
IRQ	Interrupt output	Rising/falling edge selectable
SCL/SDA	I2C	Selectable internal pull-up/open-drain mode
RST	Reset input	Low effective

surface2: Pin Description Table

Remark:

1. CMOD0/CMOD1 must be connected to a voltage stabilizing capacitor with a value between 1nF and 5.6nF;

Functional Description

CST816D self-capacitive touch chip, through its built-in fast self-capacitive sensing module, does not require any external devices (except circuit bypass capacitors).

It can realize single-point gesture and real two-point function on patterns such as triangles; while achieving fast response, it has extremely excellent noise and anti-

Water, low power consumption performance.

Power on and reset

The chip has a built-in power-on reset circuit, so there is no need to connect a dedicated reset circuit externally.

The built-in power-on reset module will keep the chip in reset state until the voltage is normal. When the voltage is lower than a certain threshold, the chip will also be reset.

When the external reset pin RST is low, the entire chip will be reset. This pin can be left floating.

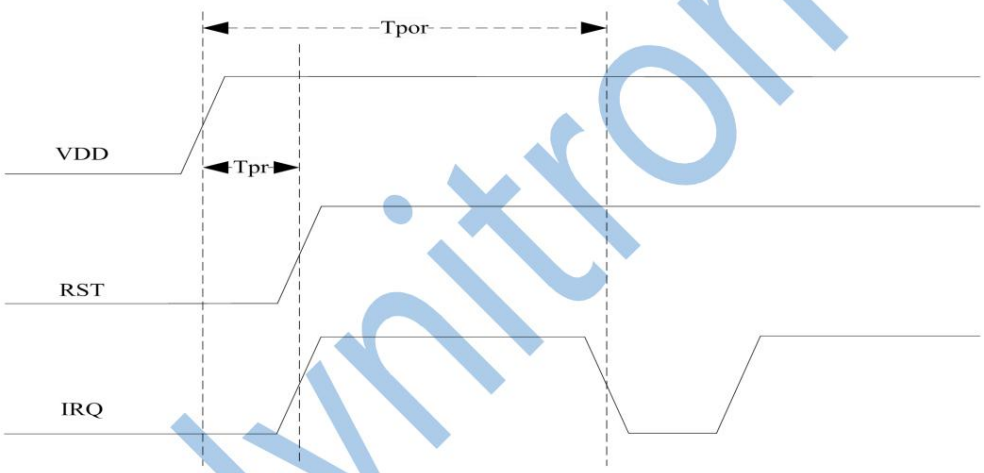


Figure 3. Power-on timing diagram

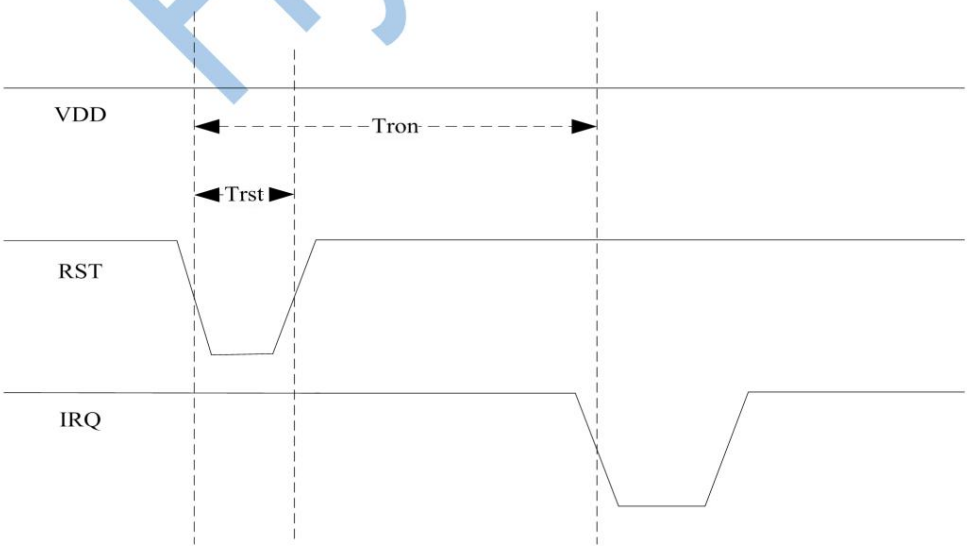


Figure 4. External reset timing diagram

symbol	describe	Minimum	Maximum	Unit
Tpor	Chip initialization time after power-on	100		mS
Tpr	RST pin high delay time	5		mS
Tron	Chip reinitialization time after reset	100		mS
Trst	reset pulse time	0.1		mS

surface 3: Power-on and reset timing description

Working Mode

Figure 5. Working mode conversion

ÿ Dynamic Mode

When there are frequent touch operations, it is in this mode; in this mode, the touch chip quickly scans the self-capacitance of the touch screen and detects Detect touch and report to the host.

After no touch for 2S, it will automatically enter standby mode. The function of automatically entering standby mode can be controlled by registers.

ÿ Sleep mode

After receiving the sleep command, it is in this mode; in this mode, the touch chip is in a deep sleep state to save power consumption to the maximum extent. Switching to dynamic mode can be done via the reset pin.

Channel/Node Configuration

Each channel of the CST816D self-capacitive touch chip can support self-capacitive scanning without external devices. The self-capacitance range supported by each channel is: 1pF ~ 400pF

I2C Communication

The chip supports the standard I2C communication protocol and can achieve a configurable communication rate of 10Khz~400Khz. The two I2C pins SCL and SDA, in addition to supporting open-drain mode, also support internal pull-up mode for flexible selection.

Interrupt mode

The touch chip notifies the host to read valid data through the IRQ pin only when it detects valid touch and needs to report it to the host, so as to improve efficiency and reduce the CPU burden; the interrupt edge can be configured as a rising edge or a falling edge as needed; when a predefined gesture is matched in standby mode, the IRQ pin is also used to wake up the host.

IIC Interface Description

The chip itself supports IIC operation, and can also use IIC pins to implement simple IO operations. Specific functions can be customized by software according to specific projects.

a) IIC address of the device

The 7-bit device address of the chip is generally 0x15, that is, the device write address is 0x2A and the read address is 0x2B.

The device addresses of some projects may be different, please consult the corresponding projects and engineering personnel.

b) IIC communication speed

In order to ensure the reliability of communication, a maximum communication rate of 400Kbps is recommended.

c) Write a single byte

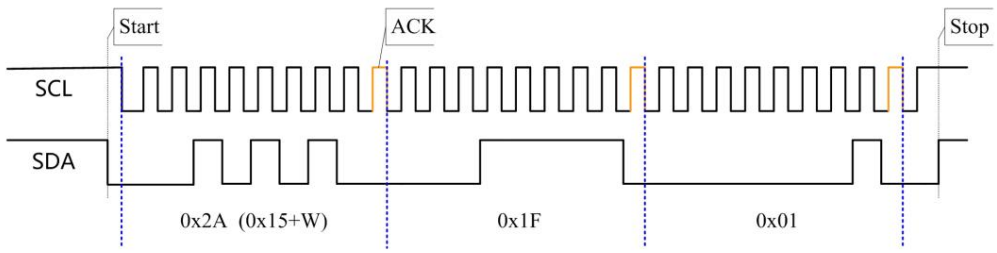


Figure 6. Past *0x1F* Register Write *0x01*

d) Write multiple bytes continuously

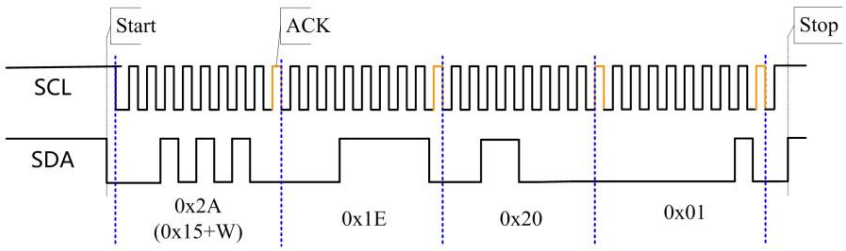


Figure 7. Past *0x1E* 、 *0x1F* Write separately *0x20* 、 *0x01*

e) Read a single byte

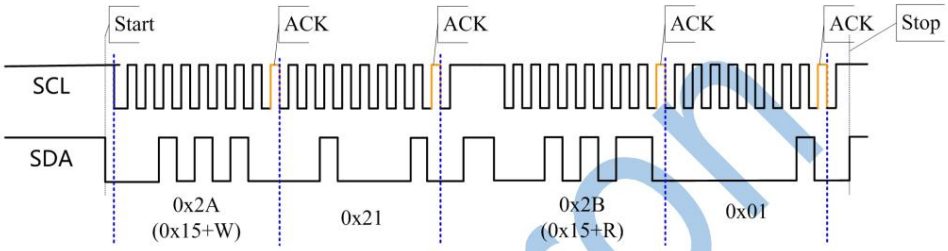


Figure 8. from *0x21* Reading a single byte

f) Read multiple bytes continuously

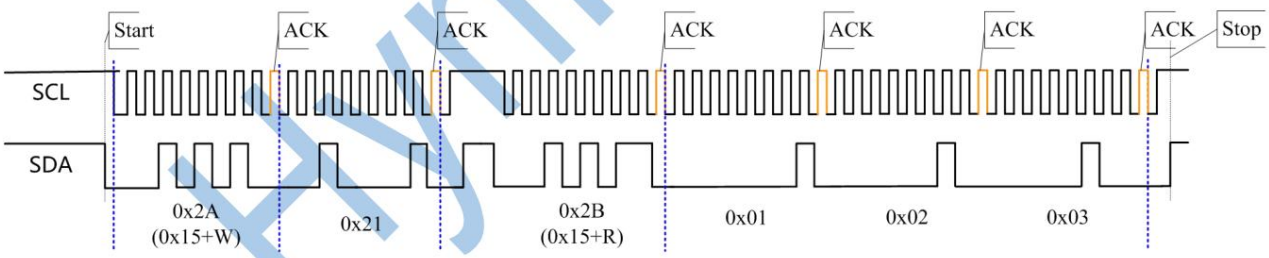


Figure 9. from *0x21* 、 *0x22* 、 *0x23* Read *3* Bytes

g) Timing Description

symbol	illustrate	Min Typ Max Unit			
F SCLI2C	I2C Clock Frequency	10		400	kHz
t HDSTAI2C	Hold time (repeated) START condition. After this period of time, the first Clock pulses	0.6			us
t LOWI2C	The low period of the SCL clock	1.3			us
t HIGHI2C	High period of SCL clock	0.6			us
tSUSTAI2C Repeated START condition setup time 0.6 tSUDATI2C Data setup time					us
		100			ns
t SUSTOI2C	STOP condition setup time	0.6			us
t BUFI2C	The total time between STOP and START conditions Line Idle Time	4.5			us

surface*4:* *IIC* Timing Description

Application Design Specifications

Power supply decoupling capacitor

Generally, a 0.1uF and 10uF ceramic capacitor connected in parallel to the VDD and VSS terminals of the chip can play the role of decoupling and bypassing. The decoupling capacitor should be placed as close to the chip as possible to minimize the current loop area.

CMOD filter capacitor

The filter capacitor uses NPO/COG material capacitors with at least 10% accuracy. The capacitance value range is between 1nF and 5.6nF, and 1nF is generally selected. The specific optimal value is related to the corresponding body capacitance. The CMOD filter capacitor must be placed close to the corresponding pin of the chip, and the trace between the chip should be as short as possible.

Waterproof precautions

There should not be large solid areas around the sensor and its wiring. Large areas of ground must be broken up.

ESD Considerations

The design of FPC will directly affect the effect of ESD. When designing, the following points must be noted: ÿ FPC should be fully shielded with magnetic film as much as possible, and the magnetic film must be grounded. ÿ The pressure and position of FPC and Sensor should be as far away from the gap of the assembly mechanism as possible to reduce the impact of ESD. ÿ Consider adding a TVS tube to the ground at the power supply access point to enhance the anti-ESD interference performance.

Electromagnetic Interference Considerations

Sensor routing must be isolated from lines that may cause interference, such as power routing, audio lines, LCD driver lines, Bluetooth antennas, RF antennas, etc. In particular, when TP adopts a full-fit design, it may be interfered by LCD, and the parameters of TP need to be specially debugged.

Ground

The high-precision detection circuit inside the touch chip is sensitive to the ground line. If possible, the user should use star grounding to isolate the noise of other chips. At the same time, insert magnetic beads in the grounding as much as possible to enhance the anti-interference ability. If star grounding is difficult to achieve, the user should also try to separate the ground of the high-current device from the ground of the touch chip.

Electrical Characteristics

Absolute Maximum Parameters

symbol	illustrate	Min Typ Max Unit			
TSTG	storage temperature	-40	25	125	ÿ
Ta	Operating environment temperature when powered on	-20		85	ÿ
Vdd	supply voltage relative to Vss	-0.3		+3.6	In
Vio	DC input voltage	VSS-0.3		VDD+0.3	In
LU	Latch-up Current		200		m.a.

surface 5: Absolute Maximum Parameters

AC electrical properties (symbols Ambient temperature 25 ÿCÿVDDA=3.3V ÿ

	illustrate	Min Typ Max Unit			
Fcpu	CPU frequency	-2%	20	+2%	MHz
F32k	internal low-speed clock frequency	-5%	32	+5%	kHz
txRST	external reset pulse width		0.1		mS
tPOWERUP	time from POR end to CPU code execution		4		mS
FGPIO	GPIO switching frequency		2		MHz
tRISE	pin level rise time, Cload=50pF tFAIL pin level fall time,		32		nS
Cload=50pF			11.2		nS

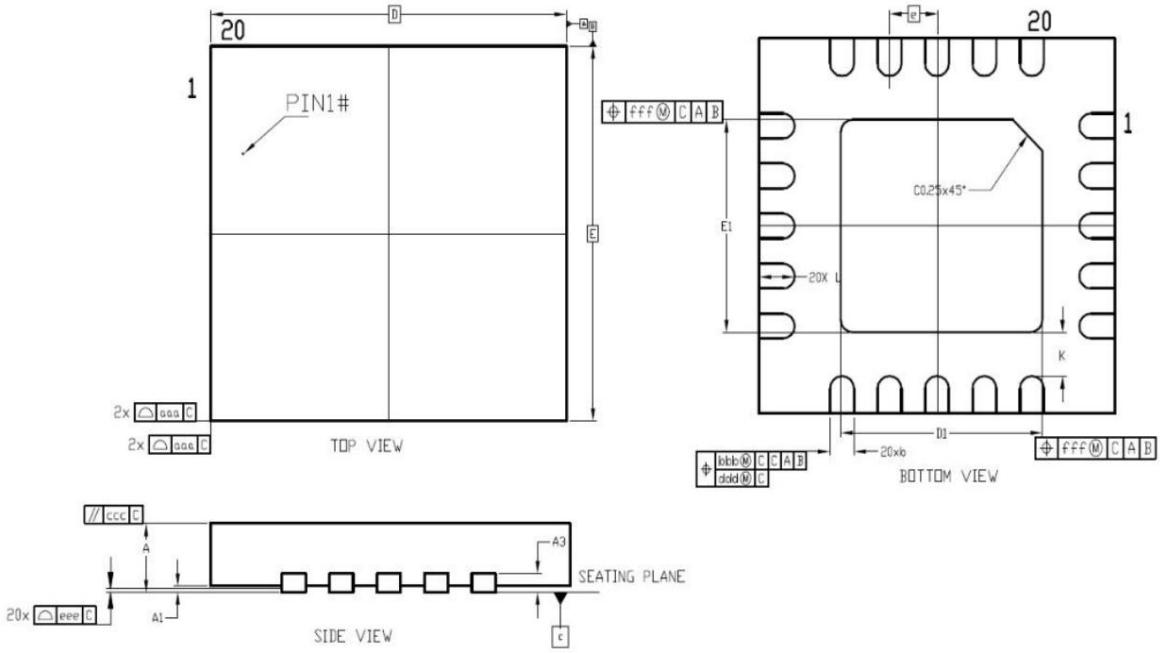
surface 6: AC electrical characteristics

DC electrical properties Ambient temperature 25 ÿCÿVDDA=3.3V ÿ

(symbols	illustrate	Min Typ Max Unit			
Vdd	supply voltage	2.8	3.0	3.6	In
Rpu	pull-up resistor		5		Kÿ
Voh	high level output voltage	0.7*Vdd			In
Vol	low level output voltage			0.3*Vdd	In
Ioh	high level output current		2.0		m.a.
Iol	low level sink current		20.0		m.a.
Vil	input low level voltage			0.3*Vdd	In
Vih	input high level voltage	0.7*Vdd			In
Iil	input leakage current		10		nA
Idd1	operating current (dynamic mode)		4.0		m.a.
Idd3	operating current (sleep mode)		8.0		a
Vddp	programming voltage	2.8		3.6	In

surface 7: DC electrical characteristics

Product Packaging



QFN20 外形图

SYMBOL / Dim	Min.	NAME.	MAX.
A	0.50	0.55	0.60
A1	0	0.02	0.05
A3	-	0.152 REF	-
b	0.15	0.20	0.25
D	3.00BSC		
AND	3.00BSC		
D2	1.60	1.70	1.80
E2	1.60	1.70	1.80
and	0.40BSC		
L	0.25	0.30	0.35
K	0.20	-	-
aaa	0.10		
bbb	0.07		
ccc	0.10		
ddd	0.05		
eee	0.08		
fff	0.10		

surface*8: QFN20* Dimensions

Revision History

版本	修订内容
V1.0	初始发行

statement

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